CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE SELECTION CIRCUITRY

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Serial No.: 08/984,562

Paragraph beginning on page 29, line 8

If mode select is active high (e.g., logic "1"), pipelined EDO mode is selected for operation of memory 100. Control logic 121 in response to receiving mode select pipelined information, provides newburst signal 110 to buffer 122 to select external input XA0-XAn. In this manner an external address via ADDR signal 115 may be sent through buffer 122 to decoder 104 for each /CAS signal 114 cycle for pipelined EDO mode. In other words, a new external column address for memory array 111 may be provided for each access to memory 100. Thus, while memory 100 is in pipelined EDO mode, newburst signal 110 instructs buffer 122 to select address inout only from ADDR signal 115.